Insight EDA Inc
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Finding Hidden Errors in Transistor-Level Design Using Analog State Analysis

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As semiconductor systems continue to grow and become more complex, circuit checking must evolve to keep pace. The number of power states in a given circuit increases, while their interactions become more nuanced. Power states define, for example: which power rails are on or off, where they are routed to, which blocks receive which power rails, and when those blocks are turned on or off.

In the latest version of the Insight Analyzer software, Insight EDA has introduced a new mode of state-based validation, called **Analog States**. It closely resembles traditional UPF (Unified Power Format) tables, but adds new enhancements and overcomes the classic limitations of UPF.

Traditional Methods

First, for the sake of comparison, this paper will discuss traditional methods used to verify transistor-level circuits. The two methods are UPF and Spice-based time-domain simulation.

UPF

UPF is an IEEE format that allows for the creation of power states to describe various combinations of states in a circuit. These power states are used to find situations when different pieces of a circuit are in incompatible states.

UPF is powerful, especially with the latest set of standards, but it has limitations in the context of circuit checking and validation. Analog bias circuits do not conform well to the terms of PST / UPF power states and control signals. Bias is a complex fabric of inter-dependent states, which cannot be supported by the “lookup table” approach of UPF. Further, analog circuits also depend on the presence or absence of voltage or current references. These are factors commonly needed to sustain a valid analog state, but simply not feasible to check with single-pass, state table methods.

SPICE Time-Domain

Time-domain simulation has universal familiarity within the industry. It too is powerful because a circuit can be simulated over time, as it transitions through states, allowing for the simulation of many

states or specific states of interest. SPICE-style simulation is also the standard for analog circuits when electrical characteristics matter more. But, time-domain analysis also has limitations: it takes time, each run must be individually configured, and there is limited cross-checking between different states, unless they are included in the same simulator run.

Analog States with Insight Analyzer

In contrast to both UPF and SPICE simulation, the new Analog States feature blends the best of both worlds to overcome their weak points. Here's how it works in the software:

1. Create Definitions: PST states are combined with contemporary analog states in a boundary table (testbench).
2. State sweeping: The relevant checks scan the circuit in multiple iterations. Before each iteration, a specific state is selected from the PST. All boundary and power settings are made as within that one specific state. (Example: Analog power is switched on, and external current reference is provided.)
3. Collating results: As the check is running through the state sweeping, violations are issued according to the particular state at hand. For example, an internal float during power down state is reported with the state name "power down" (assigned in the state definitions, in Power & States).

A crucial strength of the new Analog States feature is the ability to consider aspects such as current reference being provided in one state, then shut off (high impedance) in another state. There are other analog aspects such as regulated voltage values or bias fabric that is held by a control signal. The old "wildcard" handling of variables can not support checking of analog blocks that have multiple operating modes.

Analog States analysis is at a major advantage when there are multiple power modes applied to analog circuits. It performs multiple passes of analysis; one for each state. With traditional UPF, one pass is used to check the entire circuit, including all states.

It is important to note that Insight Analyzer still supports designs containing UPF or state table information. It can use this information to inform the circuit checking process, without extra input from the user.

About Insight Analyzer

Insight Analyzer is a full-chip, transistor-level circuit analysis tool that finds circuit design faults which a simulator / DRC / ERC can miss. Insight Analyzer intuitively understands circuit function and circuit

state, and takes the user directly to the root cause of a violation. With Insight Analyzer, a user can see a clear description of a problem and trace related parts of the violation: Driver, Receiver, DC path, etc.

The latest release of the Insight Analyzer software, v5.0, includes the new Analog States feature as well as many other circuit-checking and usability enhancements.

Comparison with Insight Analyzer v4

The previous version of Insight Analyzer, v4.9, used UPF state-based checking. A circuit was treated as a system, with states and controls defined with a UPF mindset. In this mode, all power states were available during a single pass of analysis. Several different checks, such as Domain Crossings, Power Connections, and Domain Leakage, considered UPF states if they were included in the circuit design.

UPF is commonly used in the industry, and the Analyzer's ability to consider UPF is a powerful feature. However, all the limitations of UPF described above naturally applied to this method of using it for circuit checking.

Additionally, there is a specific limitation with using UPF: checks such as Analog Floats could produce "wildcard combinations" as proposed causes of failure, without knowing that the proposal would be prevented by external factors. For example, an external current reference input might be removed, while an external disable control has not yet been asserted. While true that this would cause an internal float, the user might know that these external factors would never be presented to the circuit.

Conclusion

The new Analog States mode in Insight Analyzer v5 is powerful, and overcomes limitations of traditional UPF methods. Previous versions of Insight Analyzer performed circuit checking in a way that was more directly based on UPF. While this was still useful, the new Analog States method, with its multi-pass approach, overcomes certain drawbacks, such as with bias and reference circuits. The latest version of Insight Analyzer still fully supports UPF, and users can import UPF tables to make circuit definition more convenient.

Insight Analyzer is a full-chip, transistor-level circuit analysis tool created by Insight EDA, Inc. It is used by the world's largest IC design houses and foundries. For more information, visit insighteda.com.